Guided self-assembly of metallic nanowires and channels

B. Erdem Alaca,[a] Huseyin Sehitoglu,[b] and Taher Saif
Department of Mechanical and Industrial Engineering, University of Illinois, 1206 West Green Street, Urbana, Illinois 61801

(Received 26 January 2004; accepted 13 April 2004; published online 19 May 2004)

A method is presented to form metallic nanowires and nanochannels by guided self-assembly. The method relies on an initial plasma-enhanced chemical vapor deposition of a silicon oxide film with altered chemistry on a silicon wafer, and the cracking of the film due to tensile stresses upon annealing. The fabricated stress concentration features on the Si substrate control the number of cracks and their orientation. These cracks are then filled with electroless nickel, and the subsequent removal of SiO_2 produces a controlled network of nanowires of about 100 nm in dimension. In addition to nanowires, nanobridges, and nanocantilevers have also been fabricated by releasing the wires, confirming that the resulting structures are rather robust. © *2004 American Institute of Physics.* [DOI: 10.1063/1.1759781]

An exciting challenge in the field of nanotechnology is the synthesis of nanostructures, such as nanowires, in a cost effective manner. Currently, there are two general approaches to fabricating nanowires. In the top-down approach, highly ordered nanolines of 10 nm or higher can be patterned by electron-beam[1] or dip-pen lithography,[2] which are both slow and expensive. Cost-effective alternatives such as soft lithography[3] or nanoimprint lithography[4] can produce features as small as 25 nm provided the molds contain features at that size scale.[5] In the bottom-up approach, on the other hand, chemical reactions are initiated such that atoms or molecules self-assemble to form nanowires.[6–13] It offers cost-effective wires, but the wires are typically randomly arranged and cannot be patterned. Thus, a marriage between the two approaches resulting in patterned self-assembly is highly desirable.

Here, a rather simple method is presented for nanochannel and nanowire fabrication, where the initiation and termination points of nanostructures are prescribed, and the evolution of their pattern is dictated by stress-assisted cracking of a dielectric film on a substrate. Cracks are then used as molds for nanowires by filling them with a second material.

The very first step is to find a suitable substrate/thin film system where one can initiate cracking in the film in a controlled manner. Moreover, in the thickness direction, cracks should propagate all the way to the interface and arrest there to facilitate the filling process. Finally, crack openings should be on the order of nanometers.

The substrate/thin film system chosen for this study is Si (4-in.-diam, 450–575-μm-thick, n-doped, 1–10 Ω cm resistivity $\langle 100 \rangle$ wafers) coated with a 5-μm-thick SiO_2 film through plasma-enhanced chemical vapor deposition. The deposition parameters (Table I) are tuned to maximize silanol incorporation in the film,[14] where at elevated temperatures a condensation reaction between adjacent silanol molecules leads to escaping of water, and hence, to tensile stresses which can be estimated by measuring the wafer curvature. A KLA-Tencor Flexus Model 2908 measurement device is employed for this purpose.

Initial stress in oxide is measured to be 200 MPa in compression at room temperature. When the wafer is heated to 525 °C with a heating rate of 5 °C/min, a transition from initial compression to tensile stresses is observed. At the end of the ramp, a tensile stress of 100 MPa is recorded. Another 25 MPa is accumulated additionally, when the sample is held there for 24 h. *In situ* microscopy revealed that tensile stresses large enough to crack the film are attained within 30 min after reaching 525 °C, after which stable crack propagation takes place. Resulting cracks extend through the film thickness arresting at Si interface with minor penetration into Si.

The next issue, the selection of a suitable filler material, is solved by using Nickelex®, the electroless Ni solution by Transene Company, Inc., because of its ability to deposit on Si exposed at the crack tip and leave the SiO_2 surface intact. If properly heat treated, it also adheres well to Si.

The details of the fabrication process involve the following steps: native oxide on Si at the bottom of cracks is removed by a 10 s buffered oxide etch (BOE). Then the chip is dipped in Nickelex® solution at 95–100 °C for 2.5 min. The deposited nickel consists of independent islands that need to be fused together by heat treatment. The crack faces are widened further by BOE for 6 s. This is necessary to prevent substrate damage during the subsequent heat treatment, which is carried out at 465 °C under nitrogen flow for 2.5

TABLE I. Plasma-enhanced chemical vapor deposition parameters for SiO_2 film used in this study.

Substrate temperature	250 °C
Pressure	900 mTorr
Radio frequency power	255 mW cm^{-2}
N_2O flow rate	144 sccm
SiH_4 flow rate (5.3% SiH_4 in N_2)	110 sccm
He flow rate	320 sccm
SiO_2 deposition rate	67 nm min^{-1}

[a]Currently at: Department of Mechanical Engineering, Koc University, Rumeli Feneri Yolu, 34450 Sariyer-Istanbul, Turkey.
[b]Author to whom correspondence should be addressed; electronic mail: huseyin@uiuc.edu

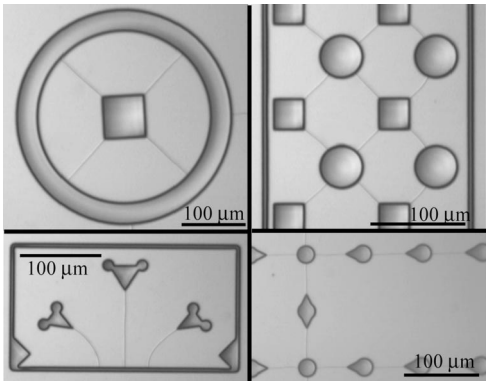

FIG. 1. Examples of self-assembled crack patterns. Triangles, squares, and circles in these examples are etched in the Si substrate through inductively coupled plasma-deep reactive ion etching prior to oxide deposition. Cracks either assume a straight path until they arrest at another etched feature (top left panel and right panels) or if the channel makes an angle with the direction of propagation of the crack, the crack diverts from its straight path and connects the channel at 90° (lower left panel).

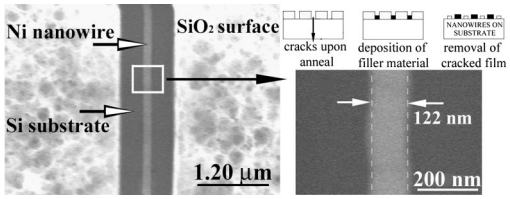

FIG. 2. Top view of a 120-nm-wide Ni line at different magnifications. The nanowire is fabricated by filling a crack in SiO_2 with Ni through electroless deposition. Requiring a Si surface, Ni deposition takes place inside cracks leaving SiO_2 surface intact. Partial removal of SiO_2 by wet etching widens the cracks and makes the underlying Si substrate visible as shown here. The inset shows the fabrication principle.

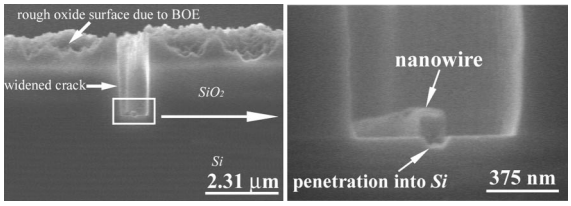

FIG. 3. Cross section of a Ni nanowire at different magnifications. The nanowire has grown on the Si substrate at the tip of a crack in SiO_2. Crack is widened in this picture by wet etching of SiO_2 after Ni deposition.

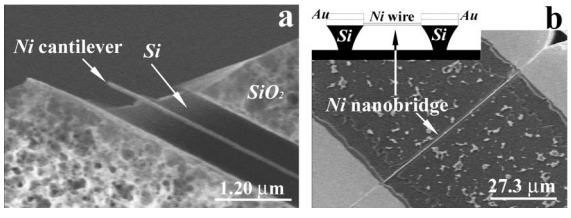

FIG. 4. (a) A released Ni wire that may serve as a probe. To ensure that the wire is partially released, a cleaved chip with the wire is inverted, placed on a plasma chamber and is subjected to SF_6 plasma for 30 s for Si etching. Si is thus etched mostly near the cleaved face, while etching inside the oxide channel is diffusion limited. (b) A 70-μm-long, free-standing nanowire bridging two gold pads. The gap between the wire and the substrate floor is 2 μm deep. The wire is in tension. The force develops as the wire is cooled to room temperature after deposition at 95 °C. A schematic of the wire is also shown.

min. Heat treatment is followed by the final Ni deposition at 95–100 °C for another 2.5 min.

Having demonstrated the principle of wire fabrication, the next issue to address is patterning, i.e., the question of dictating the number and orientation of wires. Without patterning, cracks in the film tend to propagate along ⟨100⟩ directions of the underlying Si substrate, a commonly observed phenomenon elsewhere.[15,16] Patterning is accomplished by etching sharp corners for crack initiation and free surfaces for crack termination in Si to a depth of 10 μm prior to oxide deposition via inductively coupled plasma-deep reactive ion etching through a modified Bosch process.[17] Etching of Si is followed by the deposition and annealing of the oxide film. During annealing, cracks form at the corners first, and extend along a direction that is symmetric with respect to the corner. They orient their trajectory to terminate at free edges perpendicularly such as channels or circular reservoirs in Fig. 1.

Examples of resulting wires are given in Figs. 2 and 3. Figure 2 shows a 120-nm-wide straight wire on Si. Si substrate is exposed here due to partial etching of SiO_2 in BOE for inspection purposes. The wire's cross section, shown in Fig. 3, is observed to be a square.

To obtain free-standing wires, a set of parallel wires with 20 μm spacing are also fabricated and partially released from the substrate to form 0.5-μm-long cantilevers by etching Si in SF_6 plasma [Fig. 4(a)]. Nanobridges can be fabricated similarly with Au pads on both ends. Figure 4(b) shows a 70-μm-long bridge with Si etched from underneath by 2 μm.

The implications of the proposed method are far reaching. Guided self-assembly offers a paradigm in nano fabrication where top-down and bottom-up approaches merge. The nanochannels with prescribed geometry will allow nanofluidics studies through a network of reservoirs and channels. It will also be possible to carry out fundamental studies on transport characteristics of directed nanowires. The method will thus be of interest to a variety of disciplines including biology, physics, biochemistry, and engineering.

This work was partially supported by University of Illinois' Fracture Control Program and the Department of Mechanical and Industrial Engineering in the form of Graduate Teaching Fellowship and the C. J. Gauthier Program for Exploratory Studies. Additional funding came from NSF-SGER under Grant No. ECS-0243103. Thanks to Professor David Payne and Ryan Ong for conducting the Flexus experiment and for helpful comments. Help from the staff of Micro and Nanotechnology Lab and M&IE MMS Cleanroom is gratefully acknowledged.

[1] A. M. Haghiri-Gosnet, C. Vieu, G. Simon, M. Mejias, F. Carcenac, and H. Launois, J. Phys. IV **9**, Pr2-133 (1999).
[2] R. D. Piner, J. Zhu, F. Xu, S. Hong, and C. A. Mirkin, Science **283**, 661 (1999).
[3] A. Kumar and G. M. Whitesides, Appl. Phys. Lett. **63**, 2002 (1993).
[4] Y. Chou, P. R. Krauss, and P. J. Renstrom, Appl. Phys. Lett. **67**, 3114 (1995).
[5] C. R. K. Marrian and D. M. Tennant, J. Vac. Sci. Technol. A **21**, S207 (2003).
[6] N. I. Kovtyukhova, B. R. Martin, J. K. N. Mbindyo, P. A. Smith, B. Razavi, T. S. Mayer, and T. E. Mallouk, J. Phys. Chem. B **105**, 8762 (2001).
[7] P. A. Smith, C. D. Nordquist, T. N. Jackson, T. S. Mayer, B. R. Martin, J. Mbindyo, and T. E. Mallouk, Appl. Phys. Lett. **77**, 1399 (2000).
[8] T. Thurn-Albrecht, J. Schotter, G. A. Kastle, N. Emley, T. Shibauchi, L.

Krusin-Elbaum, K. Guarini, C. T. Black, M. T. Tuominen, and T. P. Russell, Science **290**, 2126 (2000).
[9] J.-Y. Yu, S.-W. Chung, and J. R. Heath, J. Phys. Chem. B **104**, 11864 (2000).
[10] T. Hanrath and B. A. Korgel, J. Am. Chem. Soc. **124**, 1424 (2002).
[11] Y. Y. Wu, H. Q. Yan, M. Huang, B. Messer, J. H. Song, and P. D. Yang, Chem.-Eur. J. **8**, 1261 (2002).
[12] R. Djalali, Y. Chen, and H. Matsui, J. Am. Chem. Soc. **124**, 13660 (2002).
[13] M. P. Zach, K. H. Ng, and R. M. Penner, Science **290**, 2120 (2000).
[14] J. Thurn and R. F. Cook, J. Appl. Phys. **91**, 1988 (2002).
[15] L. A. Chow, Y. H. Xu, B. Dunn, K. N. Tu, and C. Chiang, Appl. Phys. Lett. **73**, 2944 (1998).
[16] L. A. Chow, B. Dunn, K. N. Tu, and C. Chiang, J. Appl. Phys. **87**, 7788 (2000).
[17] F. Laermer, A. Schilp, K. Funk, and M. Offenberg, in Proceedings of the 12th IEEE International Conference on Micro Electro Mechanical Systems, MEMS, Orlando, FL, 17–21 January, 1999, p. 211.